



1/20

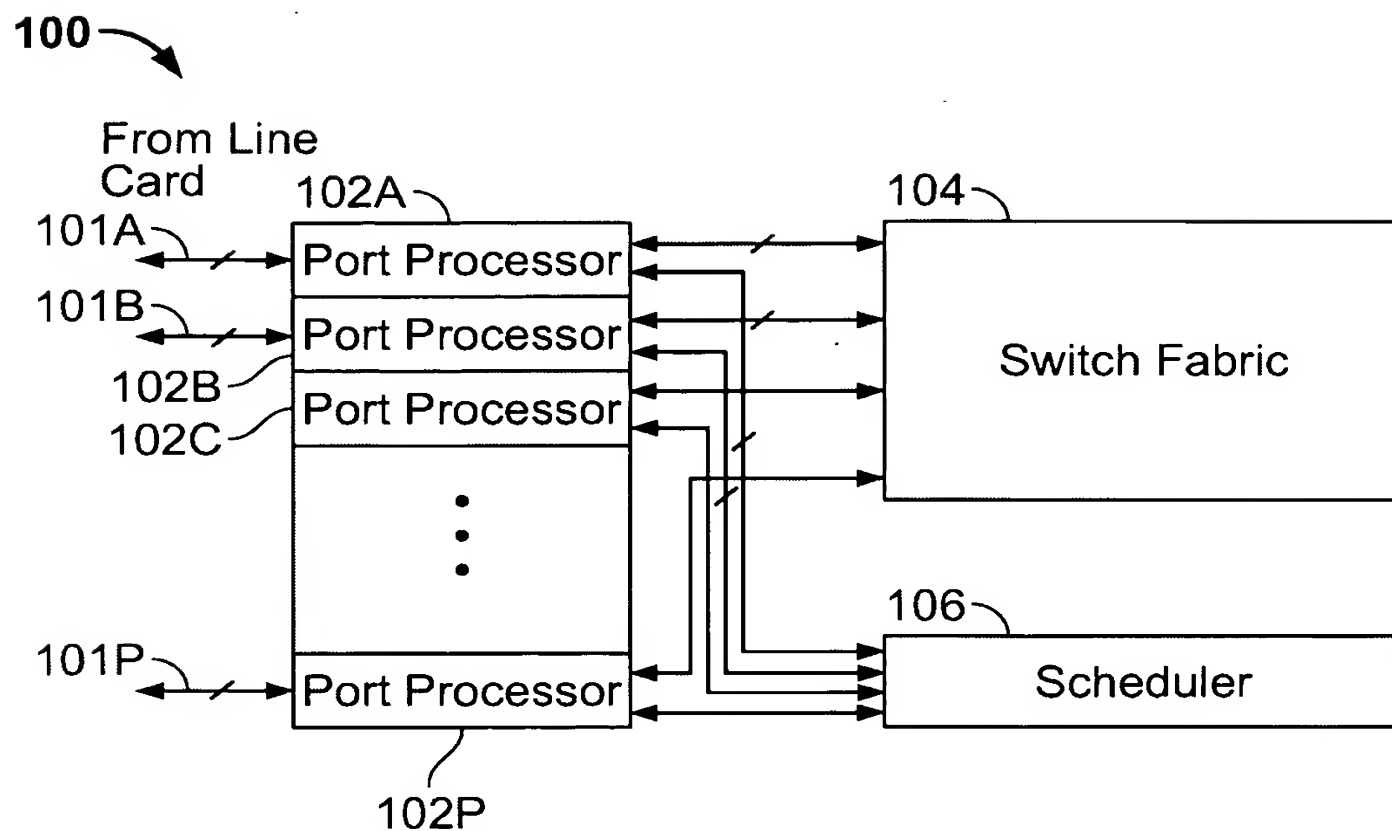


FIG. 1

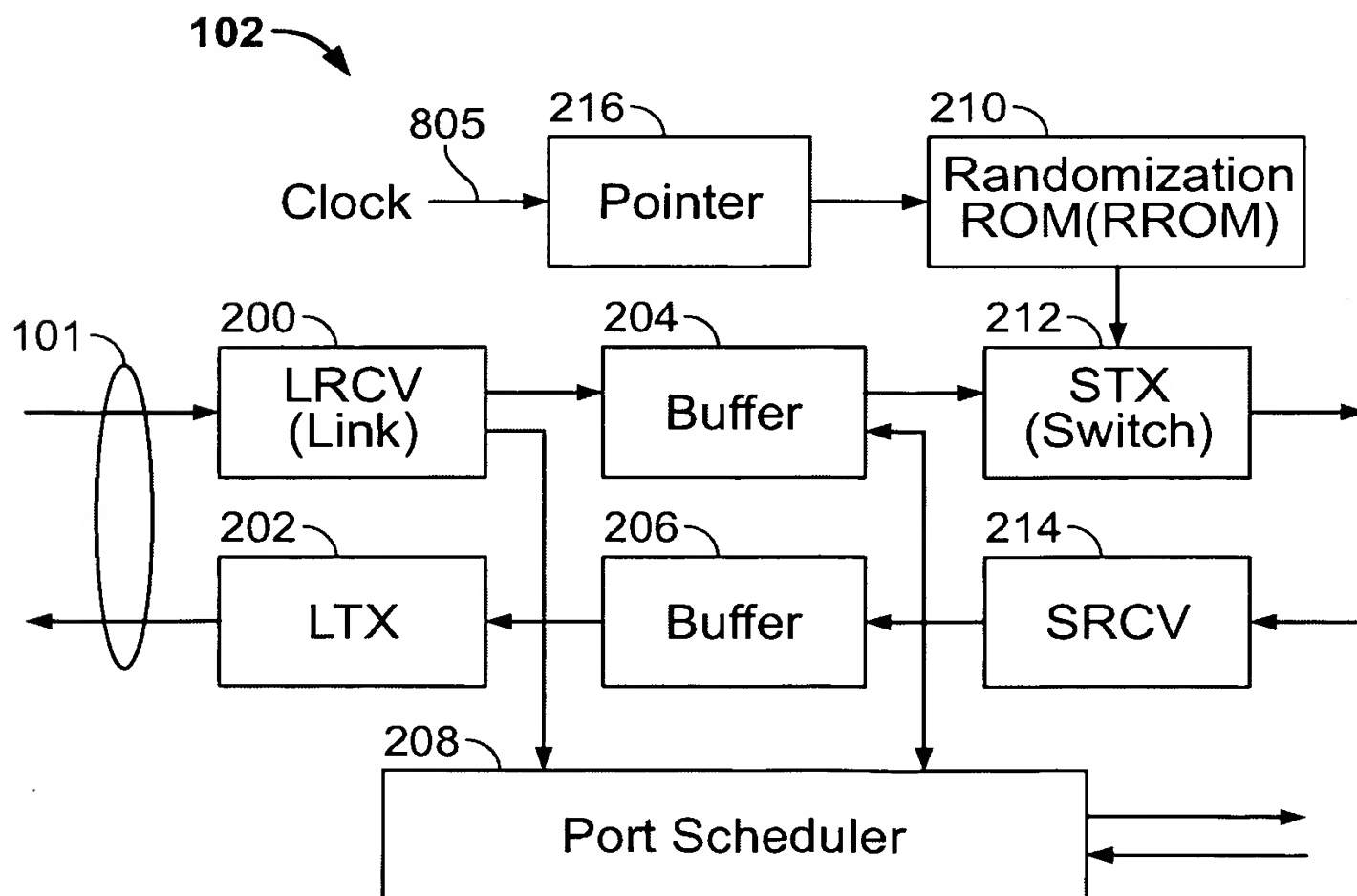


FIG. 2



2/20

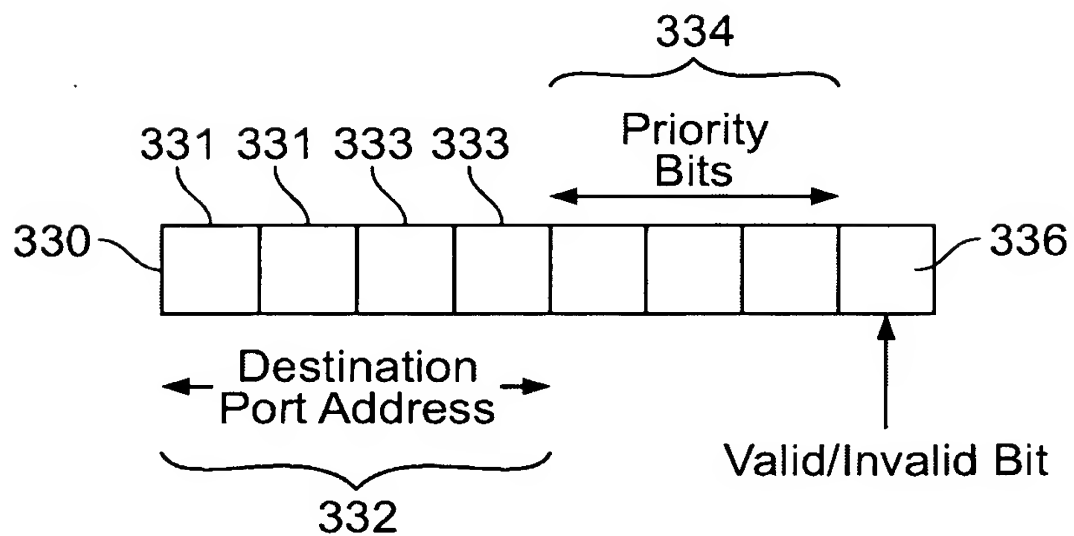


FIG. 3A

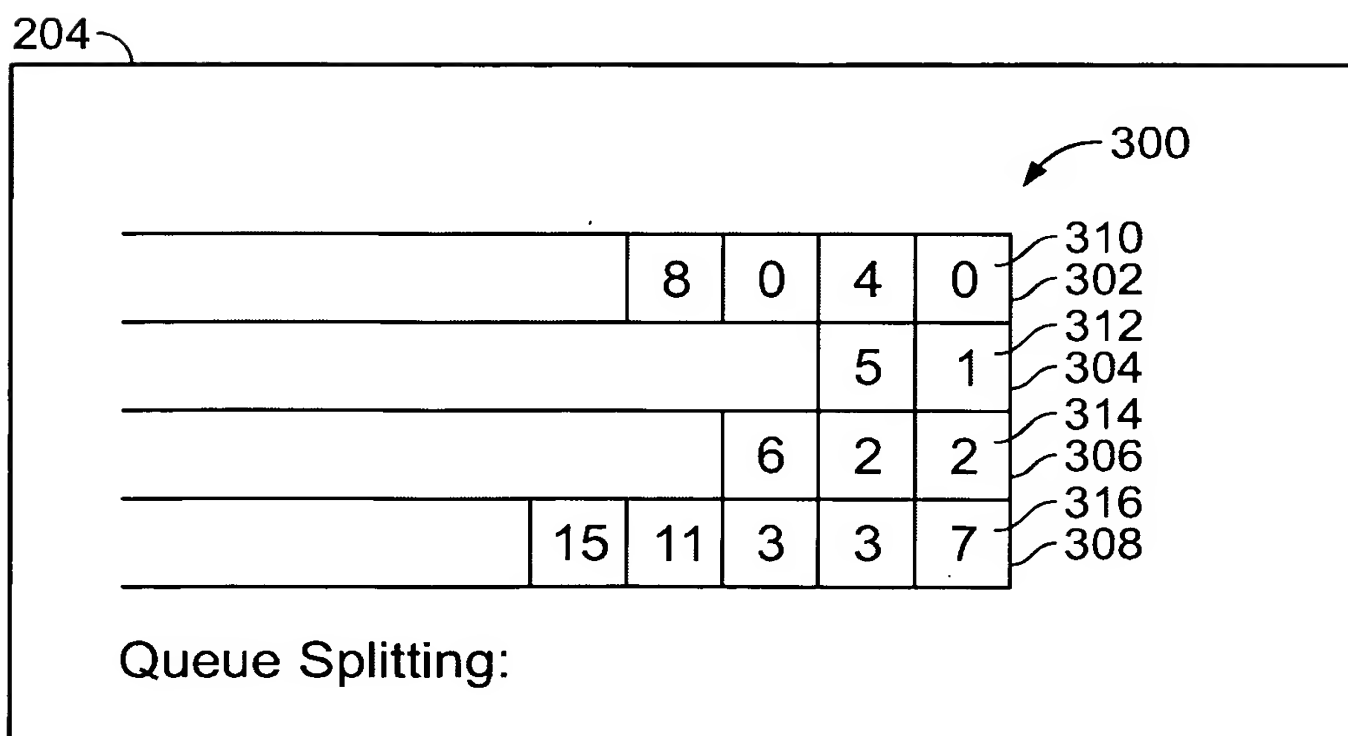


FIG. 3B



3/20

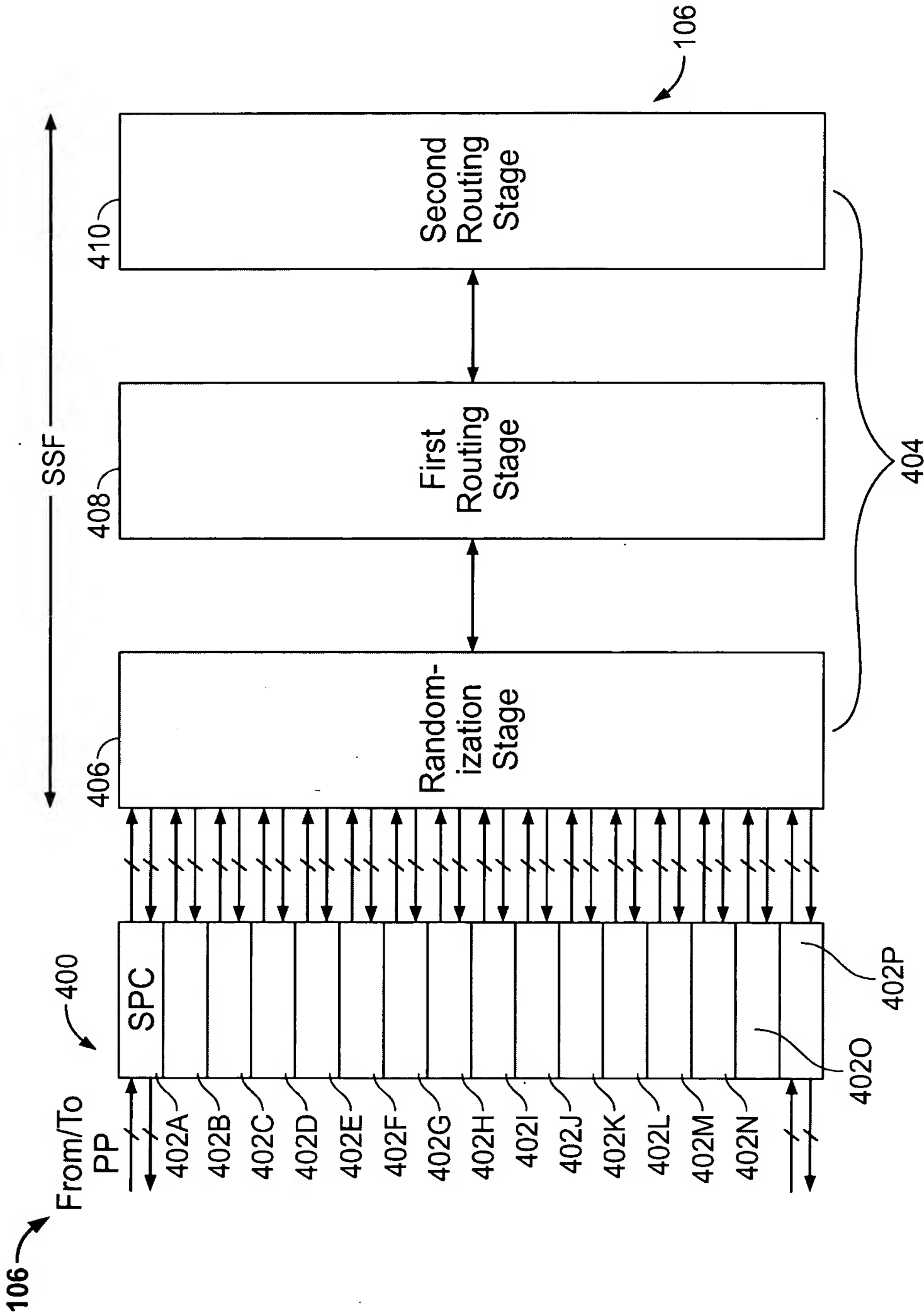


FIG. 4



4/20

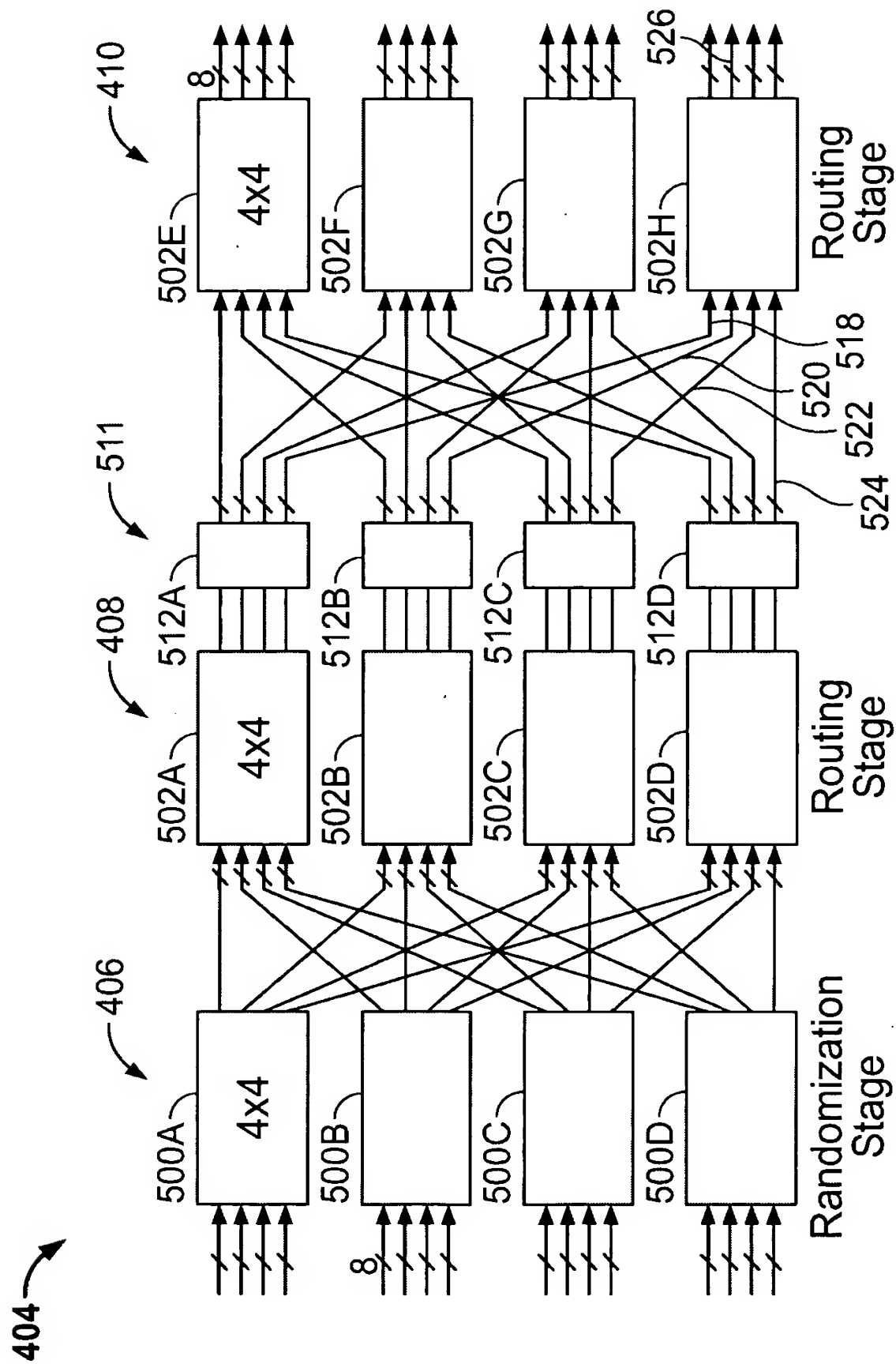


FIG. 5



5/20

500

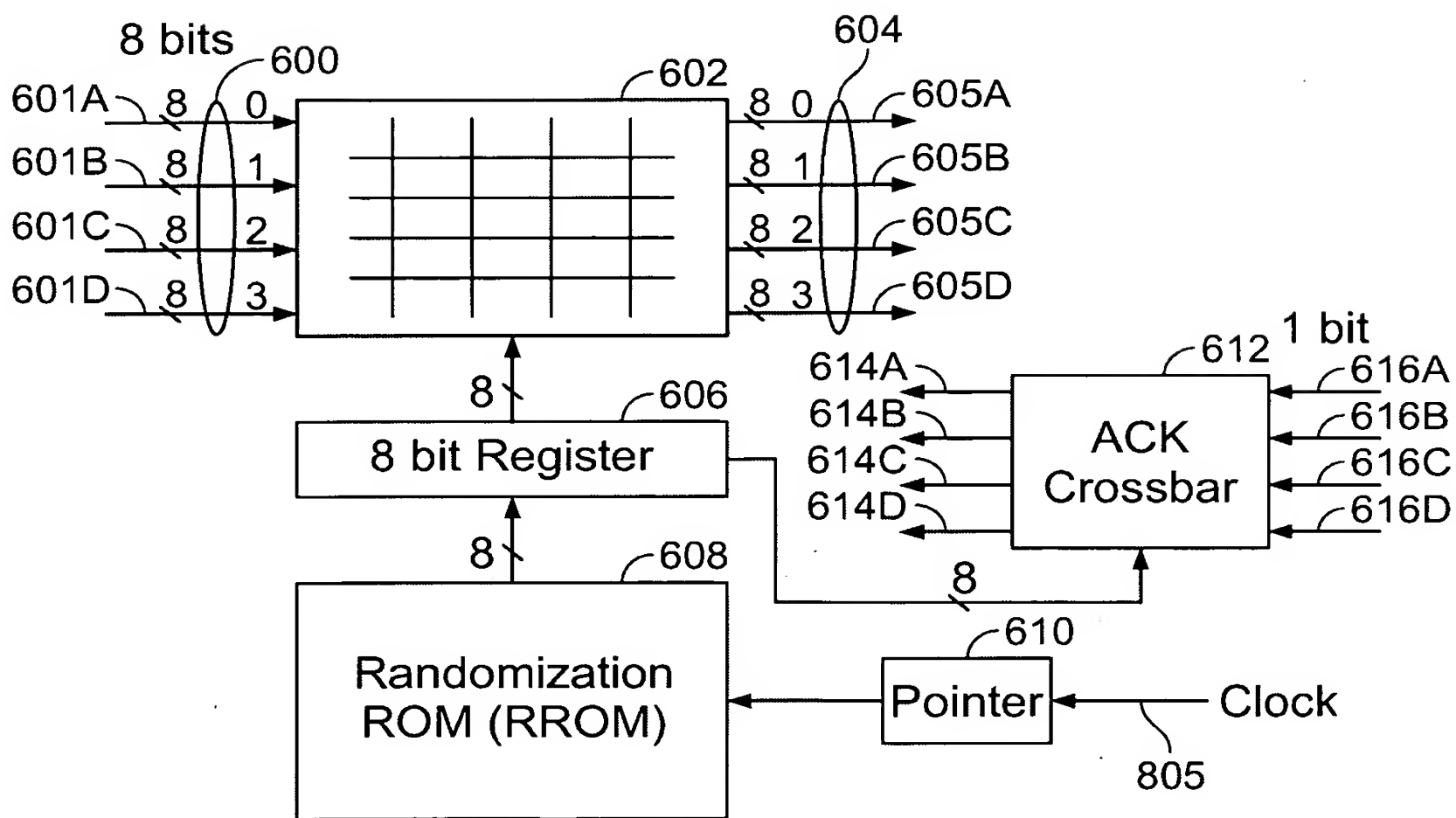


FIG. 6



6/20

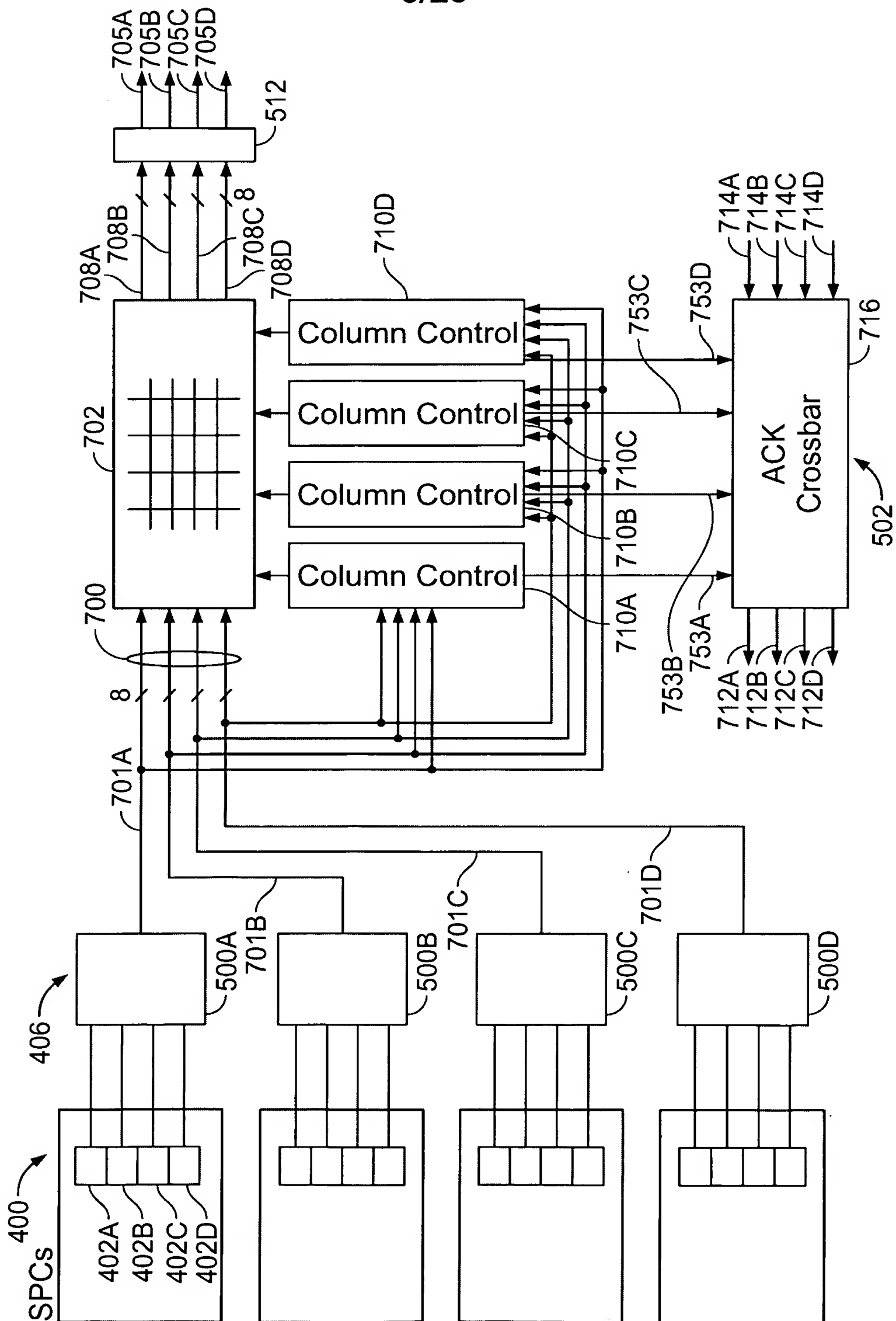
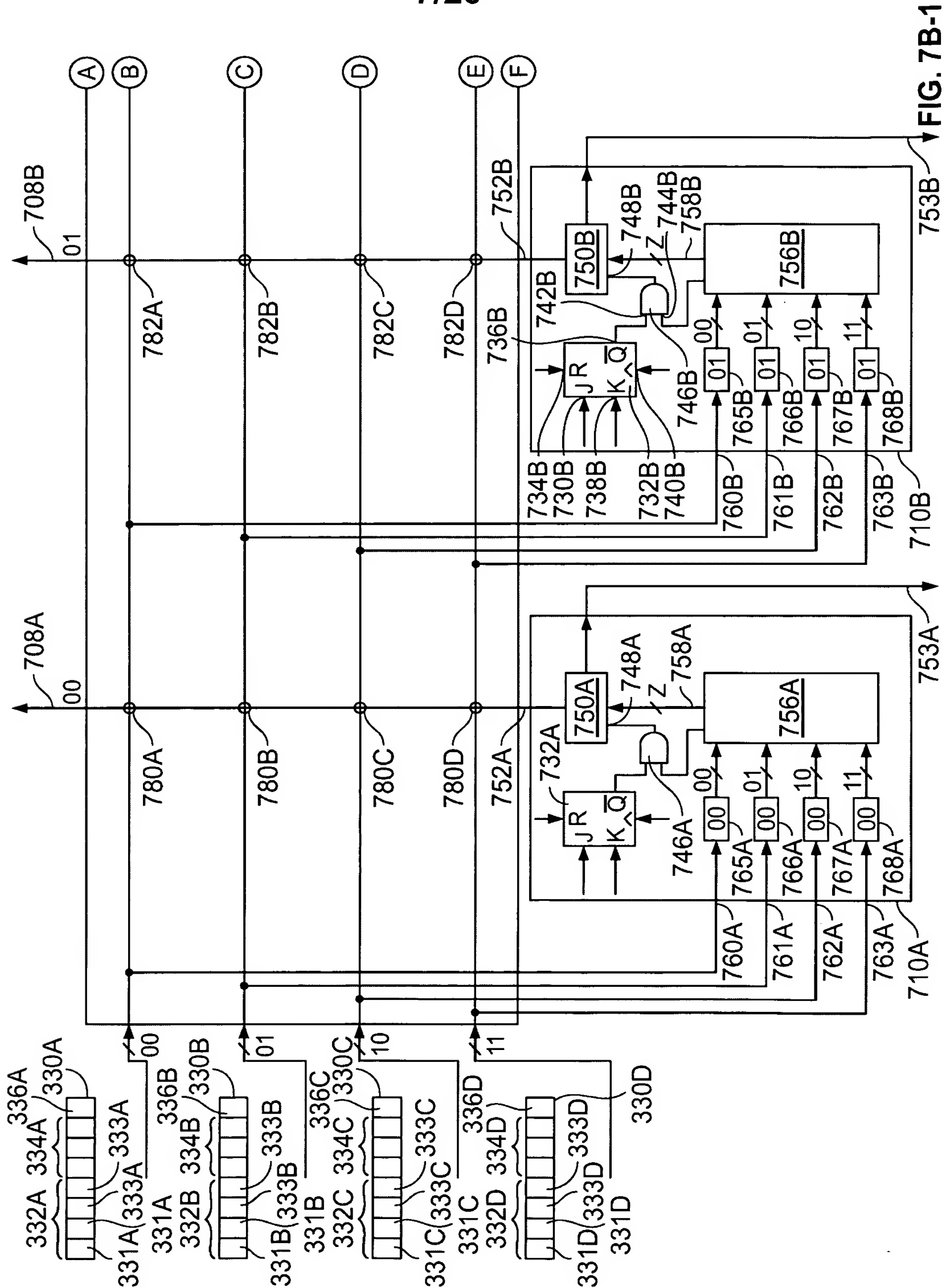
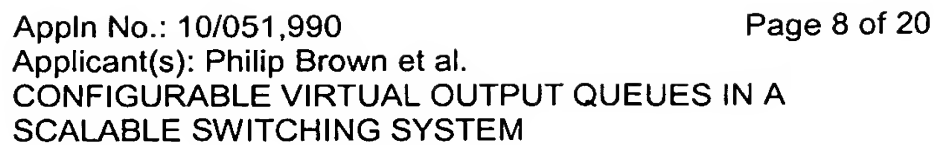


FIG. 7A

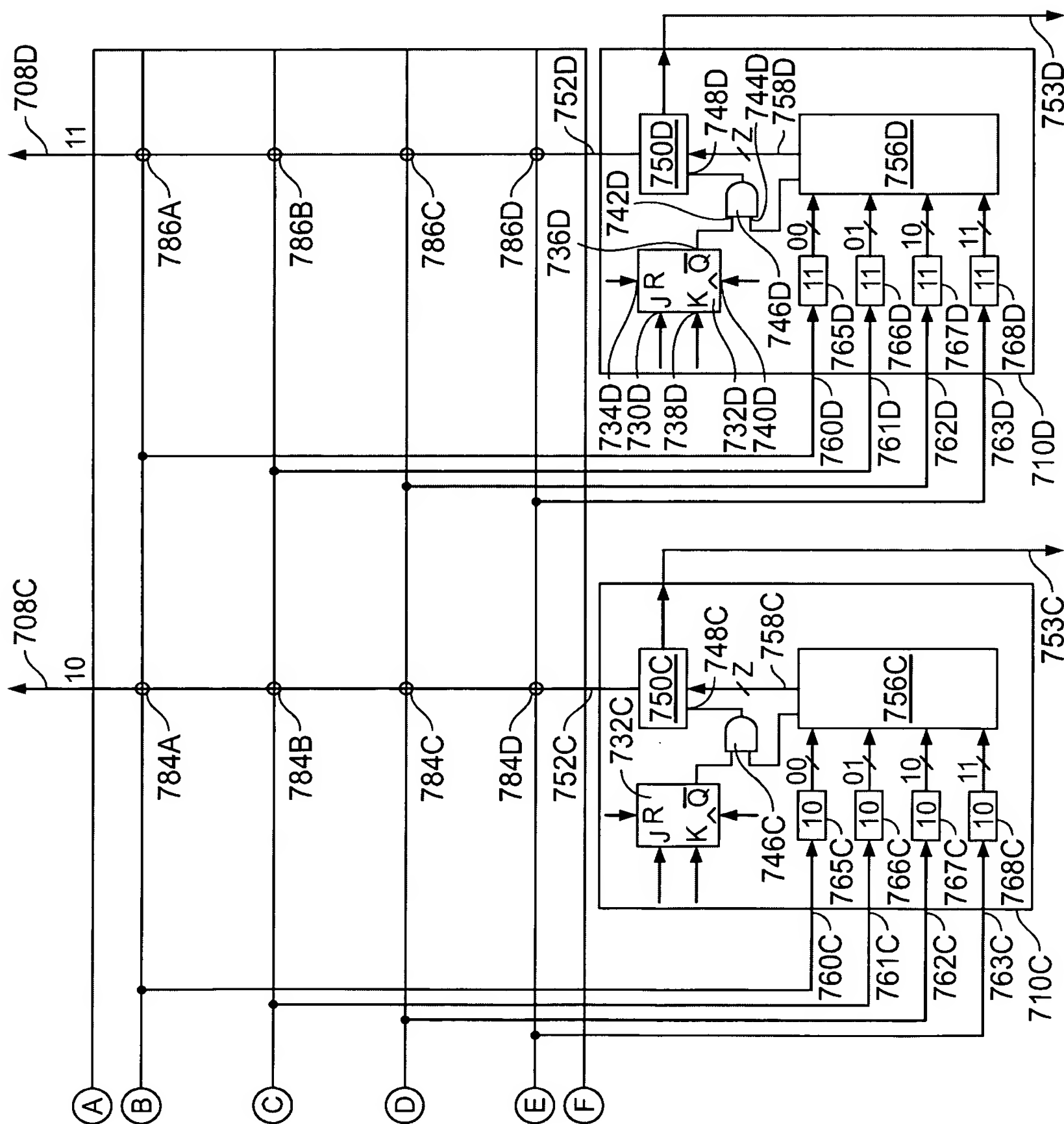


7/20



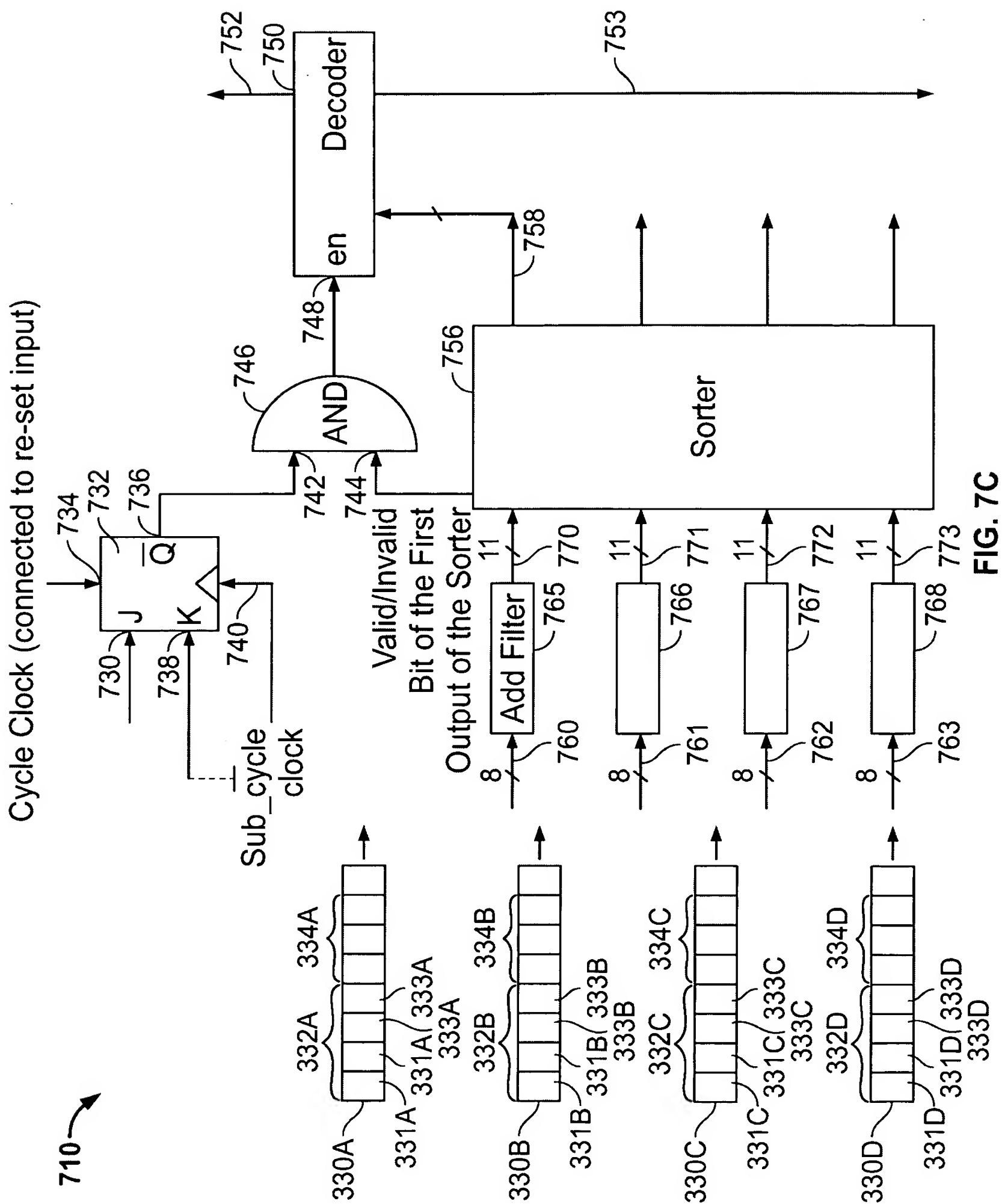


**FIG. 7B-2**





**9/20**





10/20

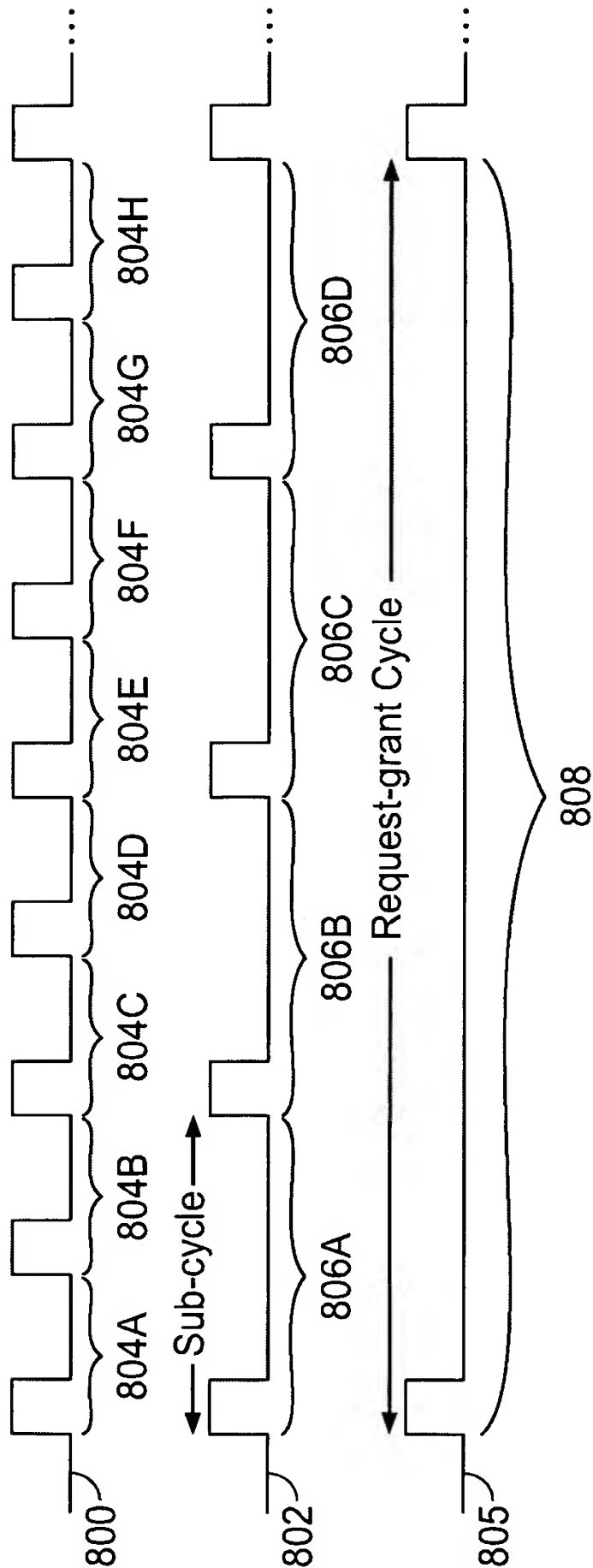


FIG. 8

11/20

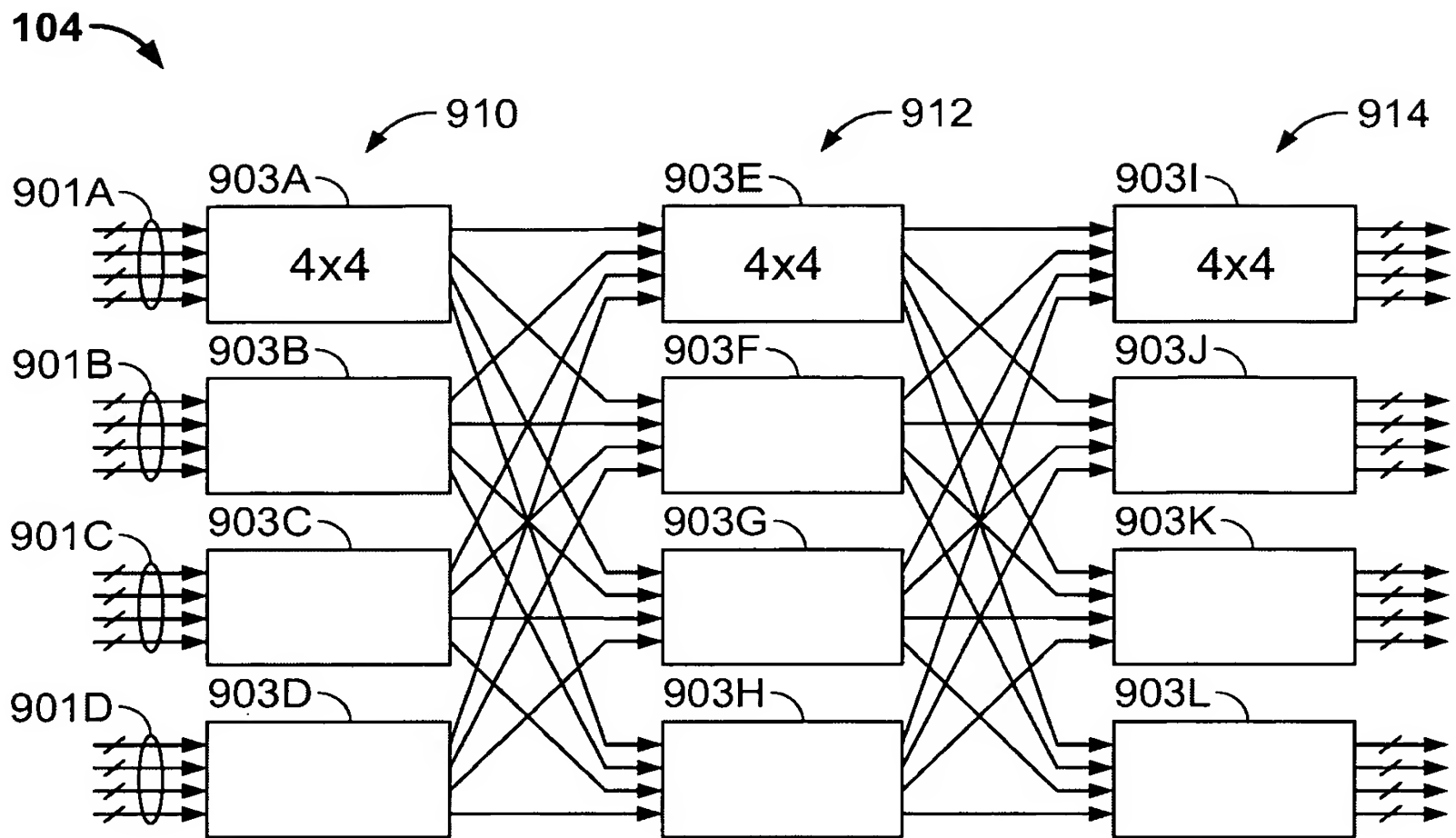


FIG. 9A

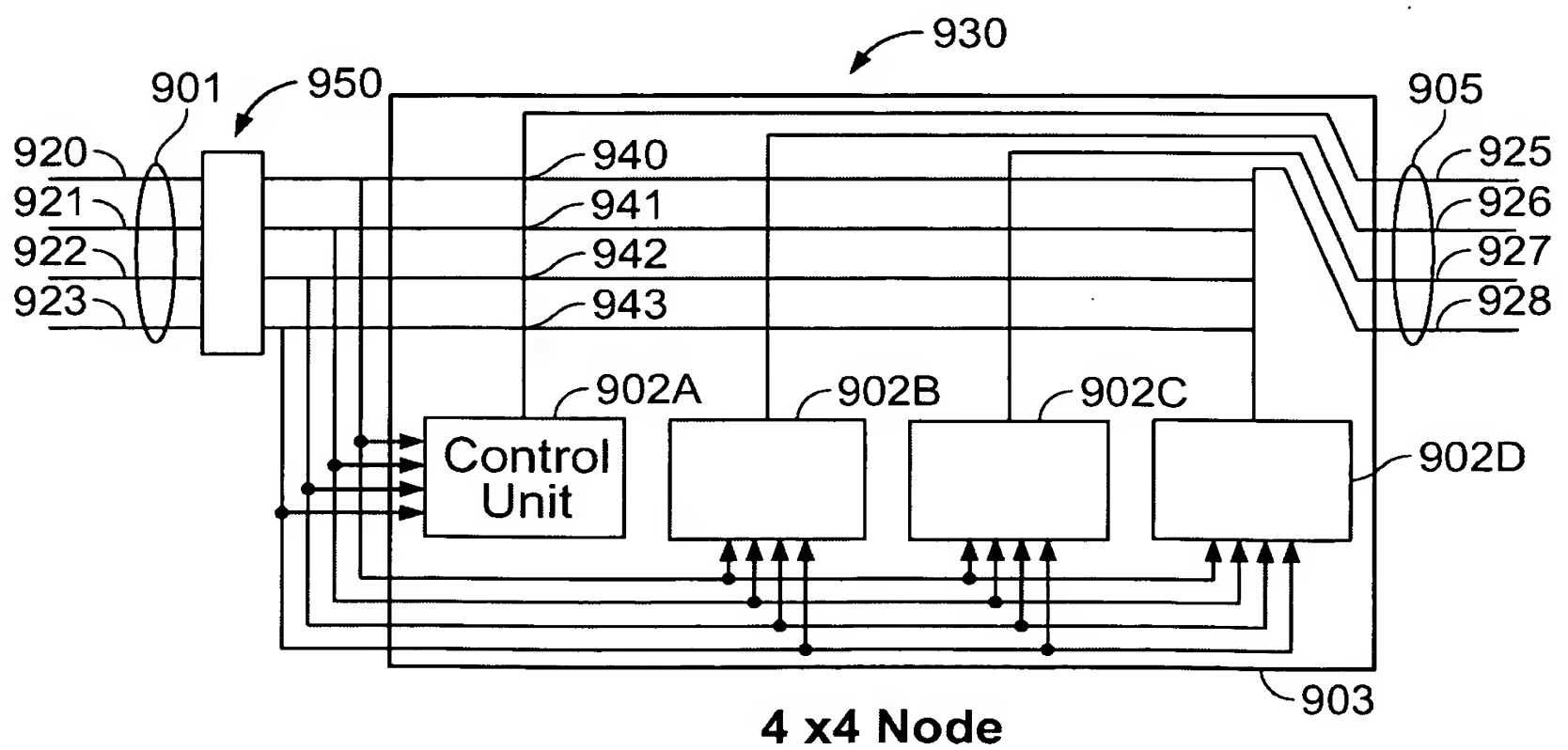
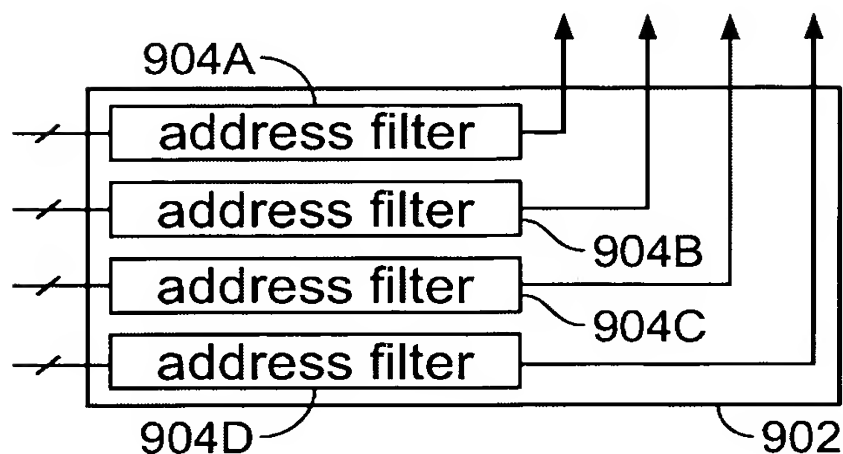


FIG. 9B



12/20



Control Unit

FIG. 9C

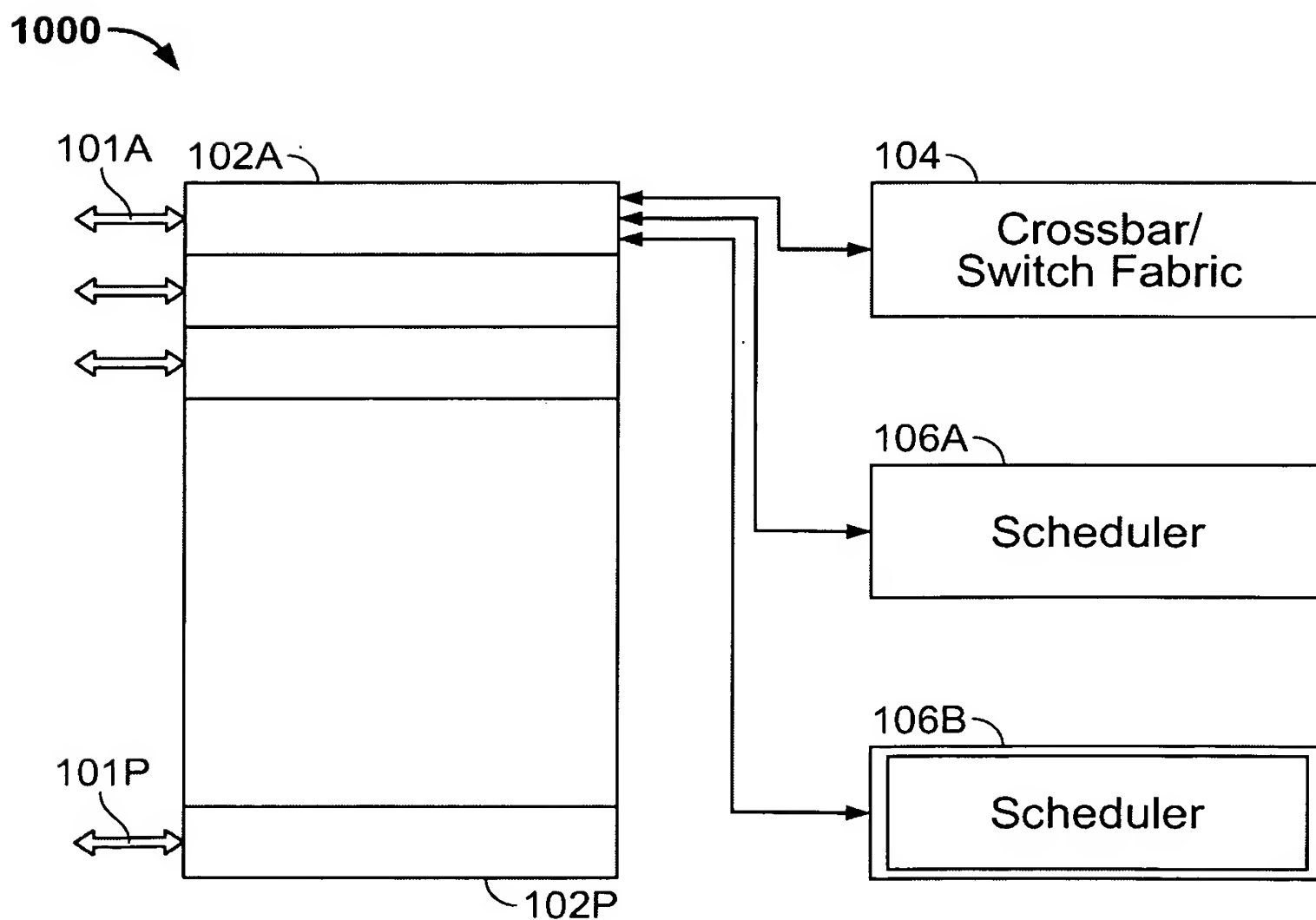


FIG. 10



13/20

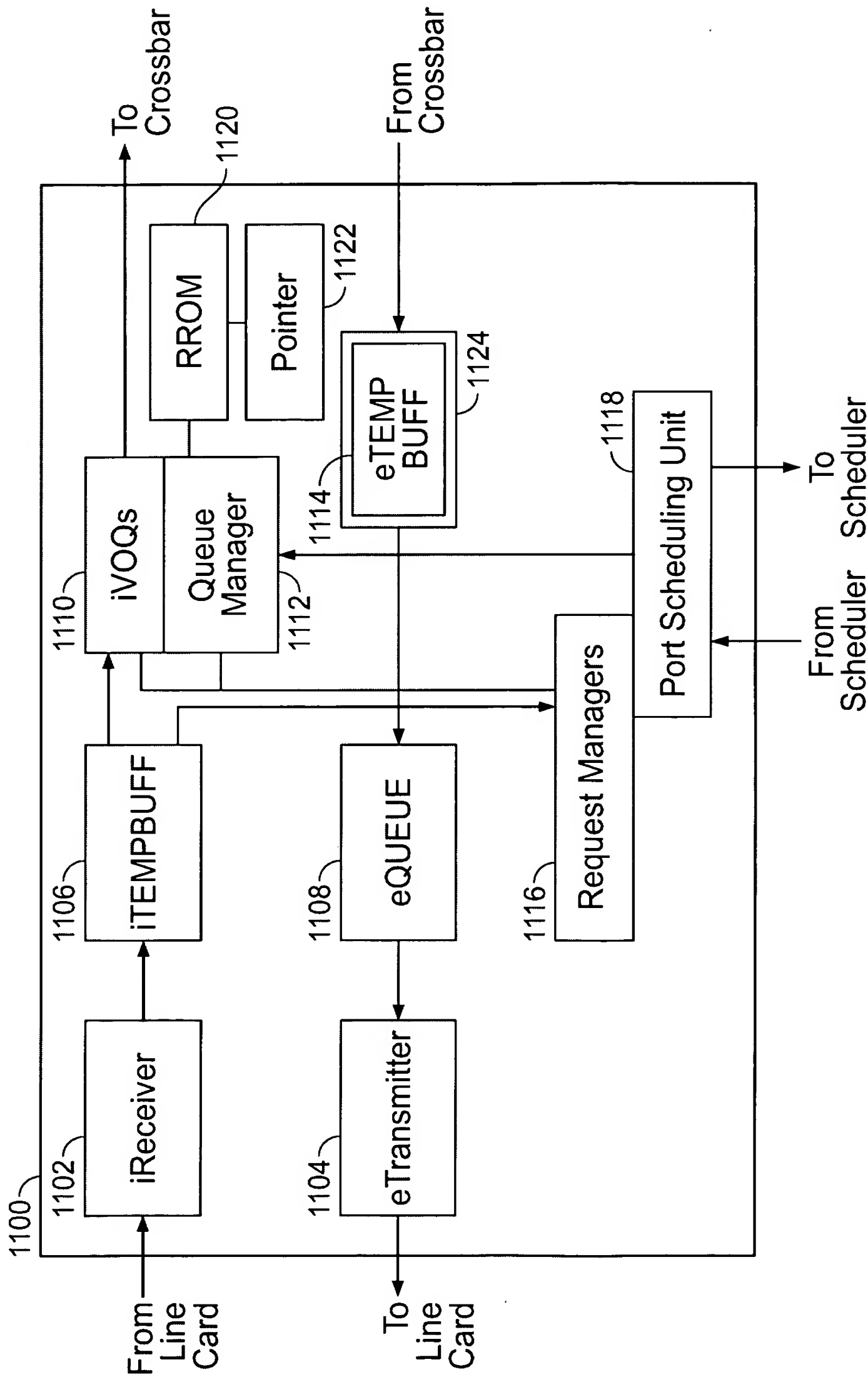


FIG. 11A



14/20

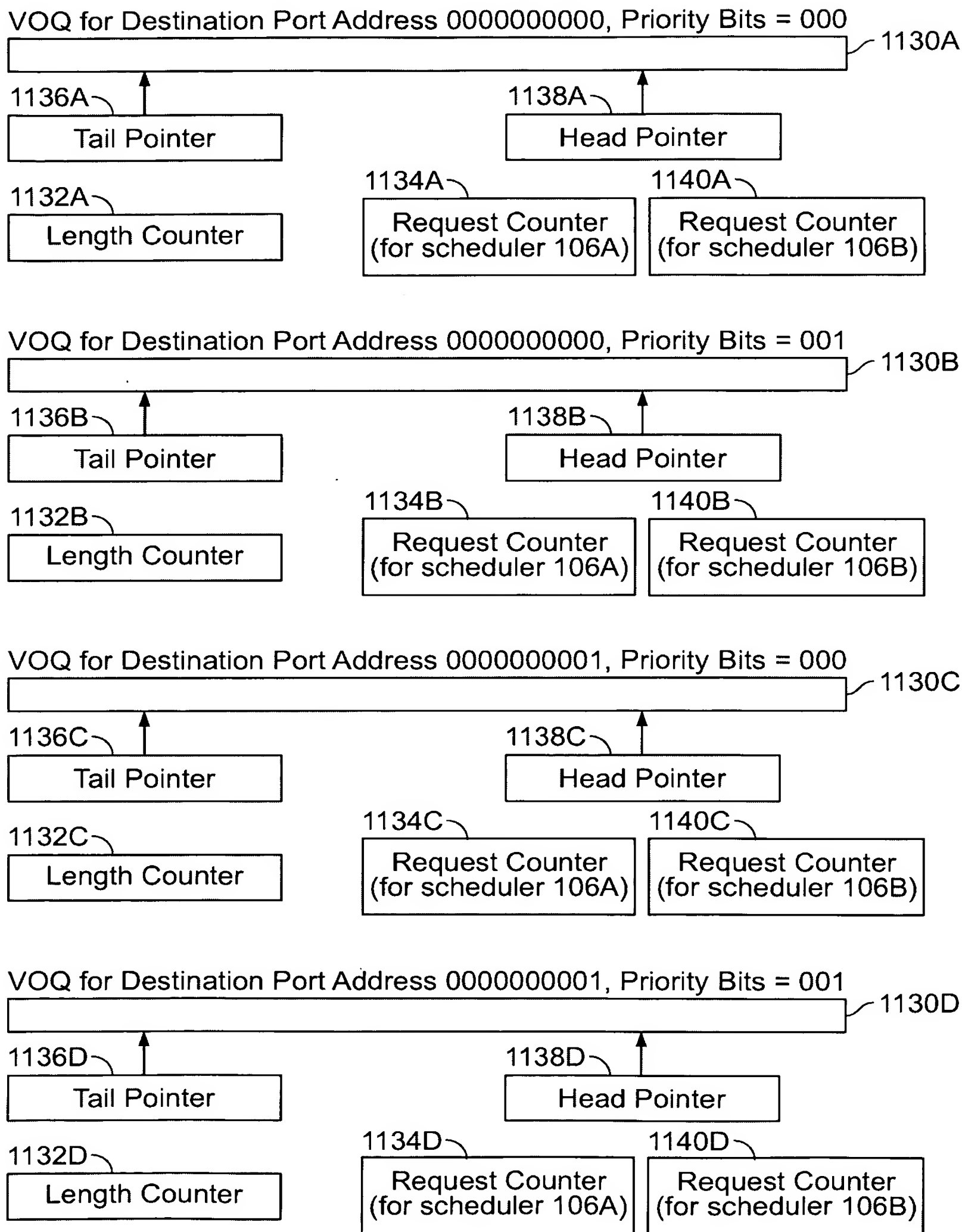


FIG. 11B



15/20

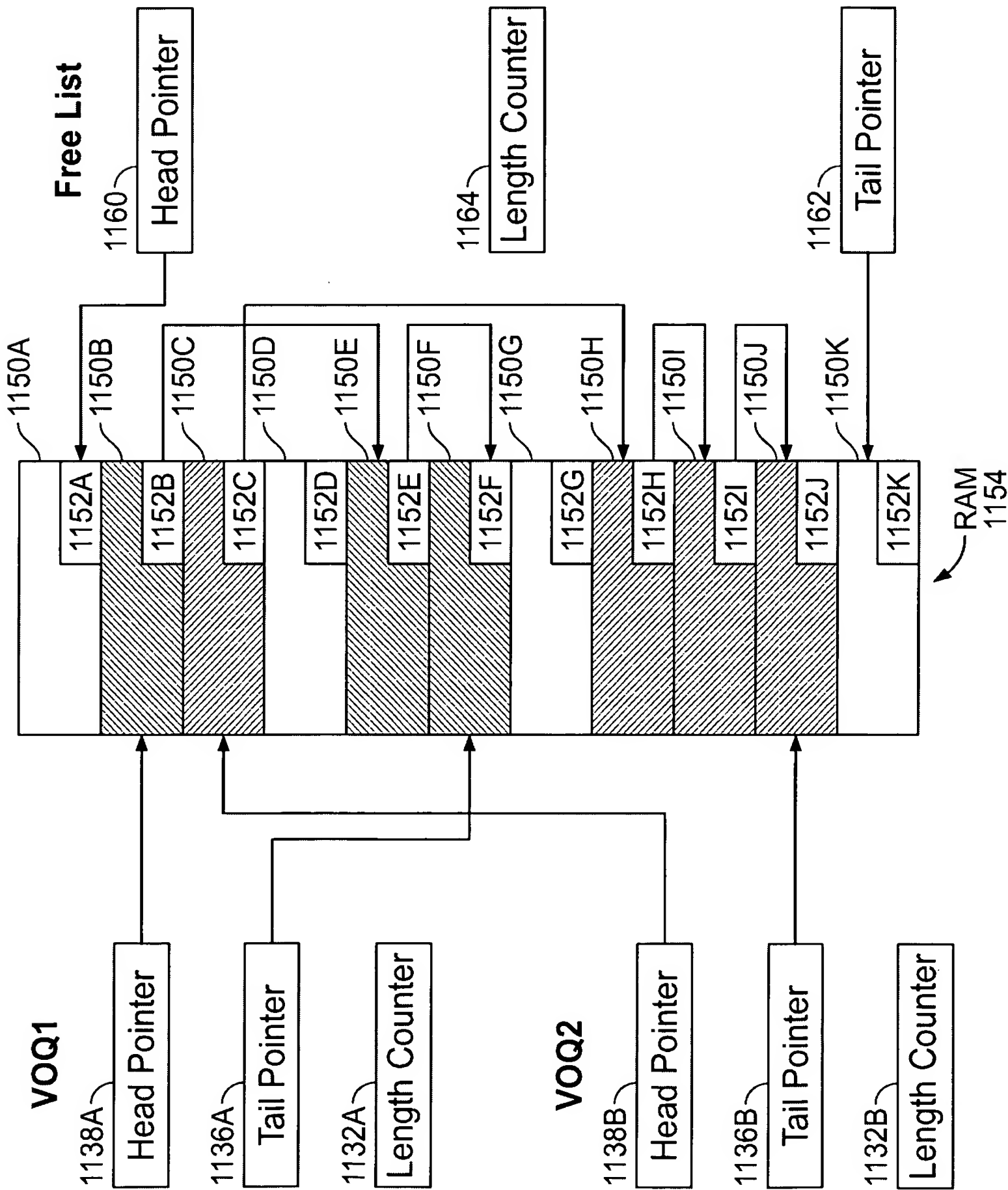


FIG. 11C



16/20

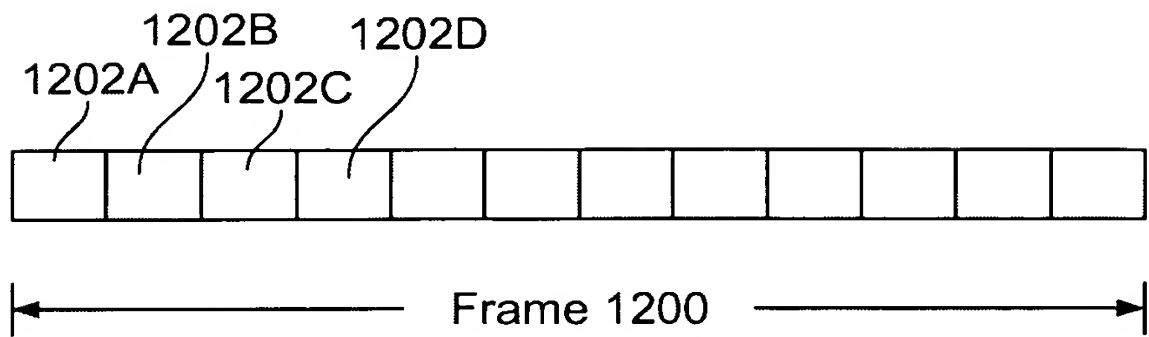


FIG. 12

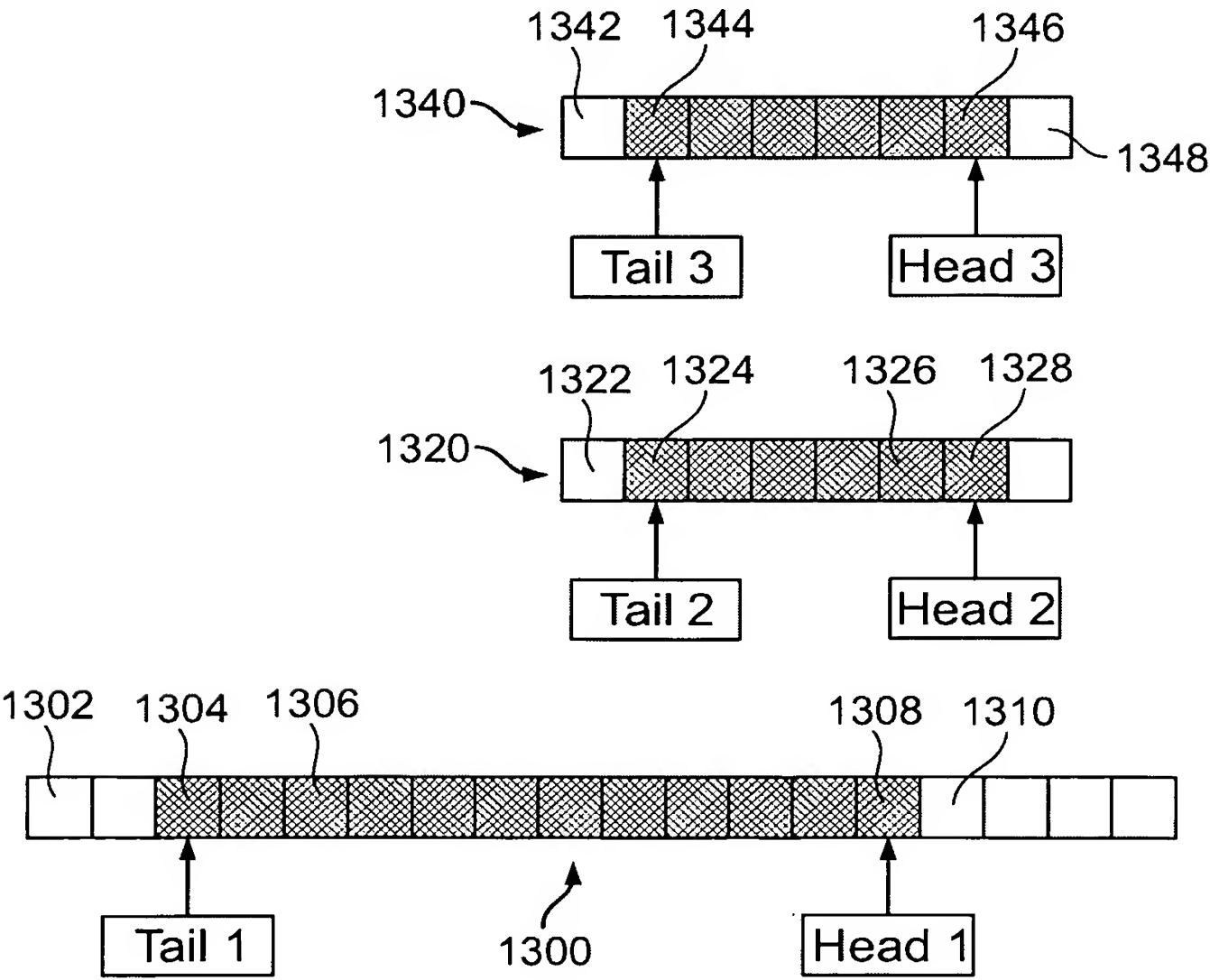


FIG. 13





17/20

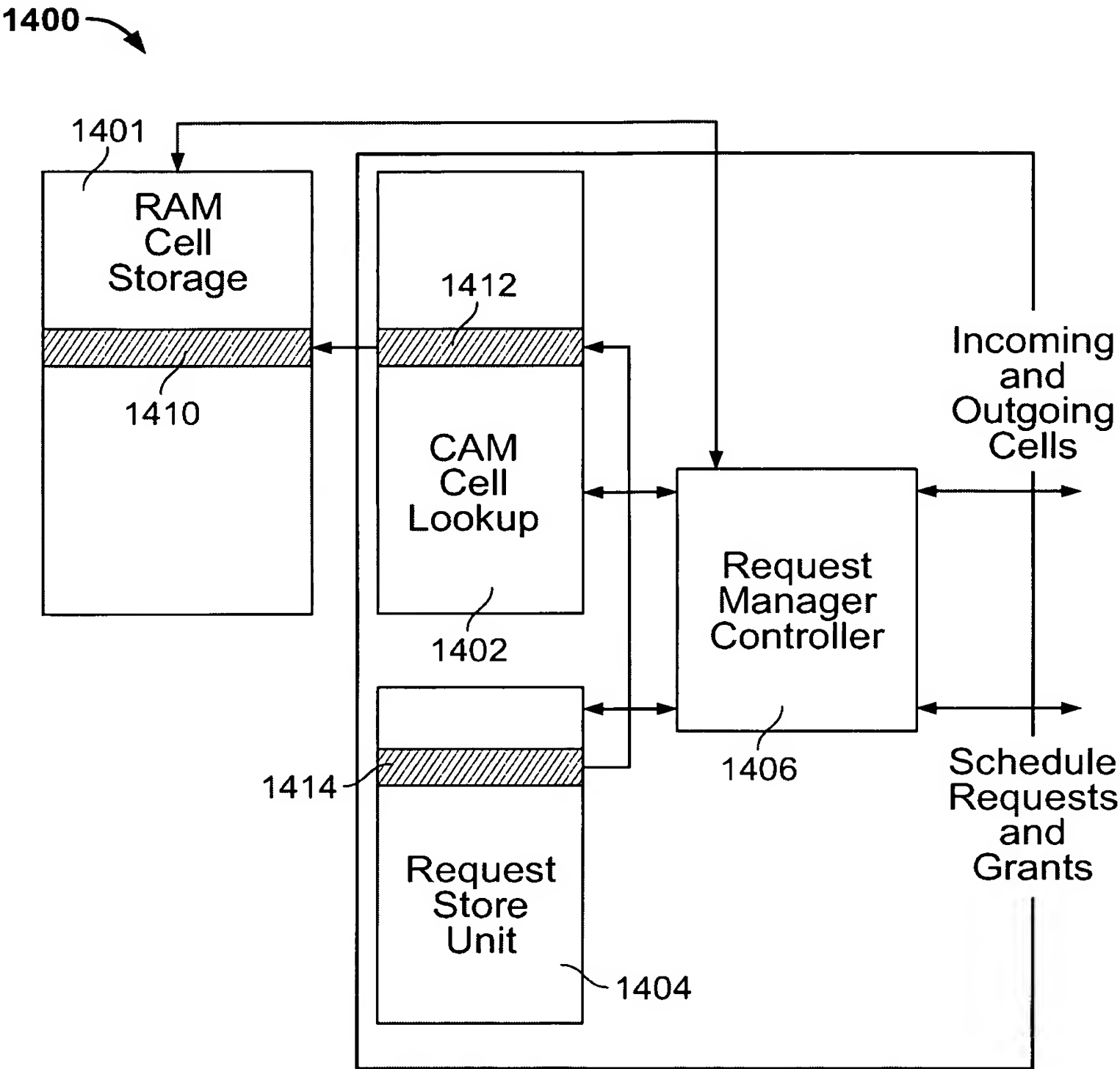


FIG. 14

Cell Lookup CAM Entry Format

Bit[0]	Valid
Bits[10:1]	Pointer
Bits[13:11]	Priority
Bits[24:14]	Destination Address

FIG. 15



**18/20**

**Unicast Request Store Entry Format**

Bit[0]	Valid
Bits[7:1]	Priority
Bits[19:8]	Destination Address0
Bits[23:20]	Request Count
Bits[33:24]	Head Pointer
Bits[43:34]	Tail Pointer
Bit[44]	Queue Over Limit
Bit[45]	Flow Control

**FIG. 16A**

Bit[0]	Valid
Bits[3:1]	Priority
Bits[15:4]	Destination Address0
Bits[19:16]	Request Count
Bits[29:20]	Head Pointer
Bits[39:30]	Tail Pointer
Bit[40]	Flow Control

**FIG. 16B**



19/20

### Multicast Request Store Entry Format

Bit[0]	Valid
Bits[3:1]	Priority
Bits[7:4]	Cell Requested
Bits[11:8]	Cell Sent
Bits[15:12]	Flow Control
Bits[25:16]	Cell Address
Bits[37: 26]	Destination Address0
Bits[49: 38]	Destination Address1
Bits[61: 50]	Destination Address2
Bits[73: 62]	Destination Address3

FIG. 17

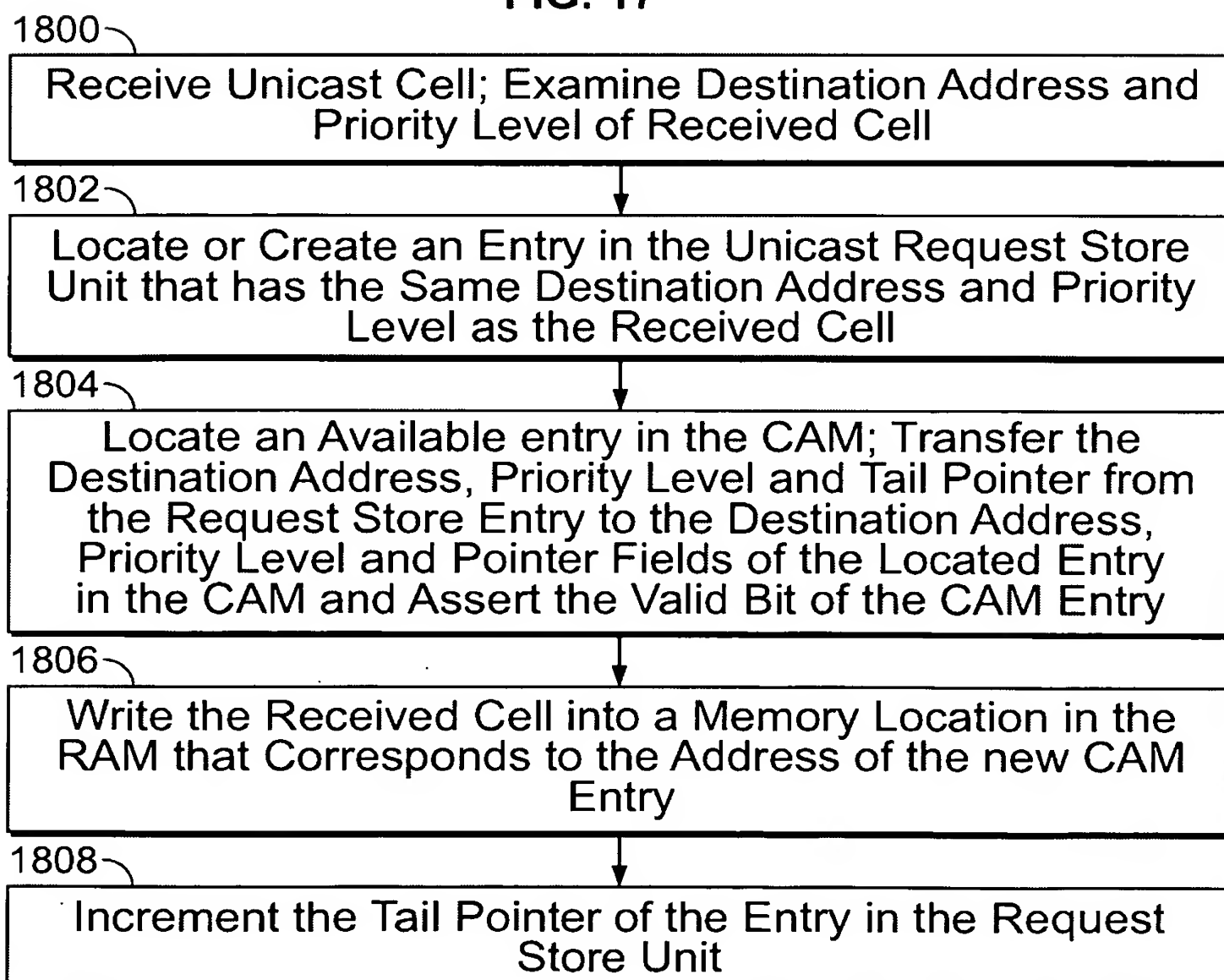


FIG. 18



20/20

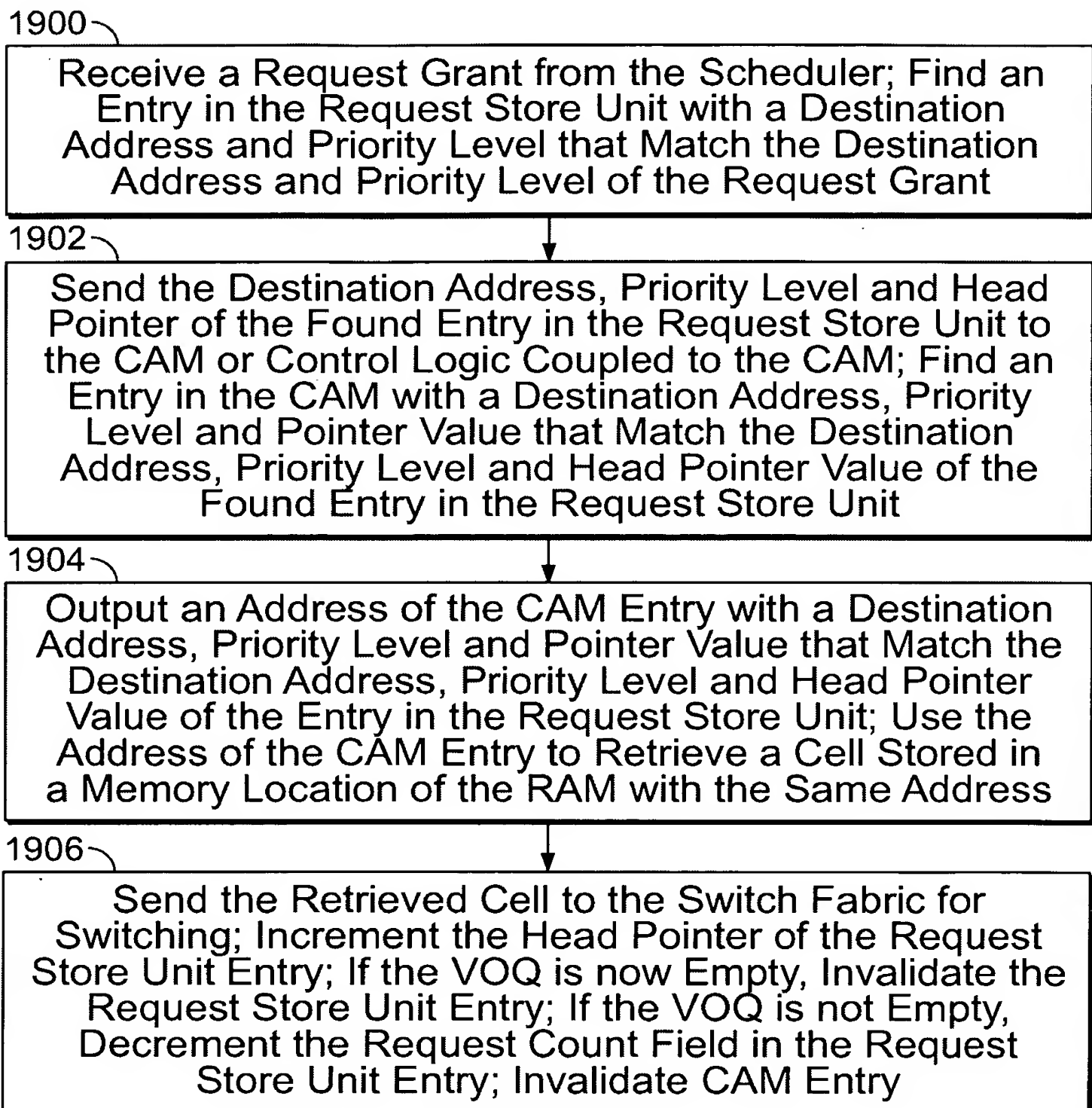


FIG. 19